Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application. In the following listing, deleted materials are crossed out and the new materials are underlined to show the amendments made.

Listing of Claims:

Claims 1-27. Previously Canceled

28. (Currently Amended) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC layout region into several sub-regions, wherein a plurality of edges exist between said sub-regions, wherein a plurality of said edges are diagonal;

b) selecting a net;

c) identifying the set of sub-regions containing the circuit elements of the selected net;

d) identifying the edges, from the plurality of edges, intersected by at least one connection graph that represents a topology of one or more interconnect lines necessary for connecting the identified set of sub-regions, wherein at least one of the identified edges is diagonal; and

e) computing a placement cost for the net by using the identified edges.

29. (Previously Amended) The method of claim 28, wherein a plurality of said edges are horizontal and a plurality are vertical.

30. (Currently Amended) The method of claim 28, wherein partitioning the IC layout region comprises using a set of partitioning lines to define said sub-regions.

31. (Previously Amended) The method of claim 30, wherein the plurality of edges are defined based on a wiring model for the IC layout and on a partitioning structure defined by the partitioning lines.

32. (Currently Amended) The method of claim 31, wherein the partitioning lines define a four-by-four partitioning grid and the wiring model is an octagonal wiring model, wherein said grid and said octagonal wiring model result in forty two edges between said sub-regions~~slots~~.

33. (Original) The method of claim 32, wherein eighteen of said edges are diagonal, and twenty-four of said edges are either horizontal or vertical.

34. (Original) The method of claim 28 further comprising:

a) changing the position of a circuit element of the selected net from one sub-region to another;

b) identifying a new set of sub-regions that contain the circuit elements of the selected net;

c) identifying a new set of edges intersected by at least one new connection graph that represents the topology of one or more interconnect lines necessary for connecting the identified new set of sub-regions; and

d) computing a new placement cost by using the identified new set of edges.

35. (Original) The method of claim 28 further comprising:

a) for each particular net, identifying the set of sub-regions containing the circuit elements of the particular net;

b) for each particular net, identifying a set of edges intersected by at least one connection graph that represents the topology of one or more interconnect lines necessary for connecting the set of sub-regions identified for the particular net; and

c) computing a placement cost for the IC layout within said region based on the identified set of edges.

36. (Original) The method of claim 35 further comprising:

a) changing the position of a particular circuit element from one sub-region to another;

b) for each particular net that includes the particular circuit element, identifying the sub-regions that contain the circuit elements of the particular net;

c) for each particular net that includes the particular circuit element, identifying a new set of edges intersected by at least one new connection graph that represents the topology of one or more interconnect lines necessary for connecting the sub-regions identified for the particular net; and

d) computing a placement cost based on the identified new edges.

37. (Original) The method of claim 35, wherein identifying the intersected edges comprises using the identity of the identified set of sub-regions to retrieve the identity of said intersected edges from a storage structure.

38. (Original) The method of claim 37 further comprising:

a) pre-computing the identity of the intersected edges for all combination of said slots; and

b) storing the computed identities in the storage structure.

39. (Original) The method of claim 28, wherein identifying the edges comprises identifying the edges intersected by all optimal connection graphs for the selected net.

40. (Original) The method of claim 39, wherein the connection graphs are determined to be optimal based on at least one particular selection criterion.

41. (Original) The method of claim 40, wherein the selection criterion is the length of the connection graphs.

42. (Original) The method of claim 41, wherein another selection criterion for determining whether the connection graphs are optimal is the number of bends of the connection graphs.

43. (Currently Amended) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC layout region into several sub-regions, wherein a plurality of line paths exist between said sub-regions, wherein a plurality of said line paths are diagonal;

b) selecting a net;

c) identifying the set of sub-regions containing the circuit elements of the selected net;

d) identifying the plurality of line paths used by at least one connection graph that represents a topology of one or more interconnect lines necessary for connecting the identified set of sub-regions, wherein at least one of the identified line paths is diagonal; and

e) computing a placement cost for the net by using the identified line paths.

44. (Previously Amended) The method of claim 43, wherein a plurality of said line paths are horizontal and a plurality are vertical.

45. (Currently Amended) The method of claim 43, wherein partitioning the IC layout region comprises using a set of partitioning lines to define said sub-regions.

46. (Original) The method of claim 45, wherein the line paths are defined based on a wiring model for the IC layout and on a partitioning structure defined by the partitioning lines.

47. (Currently Amended) The method of claim 46, wherein the partitioning lines define a four-by-four partitioning grid and the wiring model is an octagonal wiring model, wherein said grid and said octagonal wiring model result in forty two line paths between said sub-regions~~slots~~.

48. (Original) The method of claim 47, wherein eighteen of said line paths are diagonal, and twenty-four of said line paths are either horizontal or vertical.

49. (Original) The method of claim 43 further comprising:

a) changing the position of a circuit element of the selected net from one sub-region to another;

b) identifying a new set of sub-regions that contain the circuit elements of the selected net;

c) identifying a new set of line paths used by at least one new connection graph that represents the topology of one or more interconnect lines necessary for connecting the identified new set of sub-regions; and

d) computing a new placement cost by using the identified new set of line paths.

50. (Original) The method of claim 43 further comprising:

a) for each particular net, identifying the set of sub-regions containing the circuit elements of the particular net;

b) for each particular net, identifying a set of line paths used by at least one connection graph that represents the topology of one or more interconnect lines necessary for connecting the set of sub-regions identified for the particular net; and

c) computing a placement cost for the IC layout within said region based on the identified set of line paths.

51. (Original) The method of claim 50 further comprising:

a) changing the position of a particular circuit element from one sub-region to another;

b) for each particular net that includes the particular circuit element, identifying the sub-regions that contain the circuit elements of the particular net;

c) for each particular net that includes the particular circuit element, identifying a new set of line paths used by at least one new connection graph that represents the topology of one or more interconnect lines necessary for connecting the sub-regions identified for the particular net; and

d) computing a placement cost based on the identified new line paths.

52. (Original) The method of claim 50, wherein identifying the line paths comprises using the identity of the identified set of sub-regions to retrieve the identity of said line paths from a storage structure.

53. (Original) The method of claim 52 further comprising:

a) pre-computing the identity of the line paths used for all combination of said slots; and

b) storing the computed identities in the storage structure.

54. (Original) The method of claim 43, wherein identifying the line paths comprises identifying the line paths used by all optimal connection graphs for the selected net.

55. (Original) The method of claim 54, wherein the connection graphs are determined to be optimal based on at least one particular selection criterion.

56. (Original) The method of claim 55, wherein the selection criterion is the length of the connection graphs.

57. (Original) The method of claim 56, wherein another selection criterion for determining whether the connection graphs are optimal is the number of bends of the connection graphs.

58. (Currently Amended) For an electronic-design-automation placer that uses a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions corresponding to said slots, wherein a plurality of line paths exist between said slots, a method of pre-computing attributes that are used for ~~costs of~~ placing circuit modules in an IC layout region, the method comprising:

a) for each combination of said slots, identifying at least one connection graph that represents a topology of interconnect lines necessary for connecting the combination of said slots;

b) for each combination of said slots, identifying the line paths used by the connection graph or graphs for that particular combination of slots, wherein a plurality of the identified line paths are diagonal; and

c) storing the plurality of identified line paths for each combination of slots in a storage structure, wherein said stored line paths are used by the placer to compute costs associated with different placements.

59. (Previously Amended) The method of claim 58, wherein a plurality of the line paths are horizontal, and a plurality are vertical.

60. (Original) The method of claim 58, wherein the connection graphs are Steiner trees.

61. (Original) The method of claim 58, wherein the connection graphs are minimum spanning trees.

62. (Original) The method of claim 58, wherein identifying the line paths comprises identifying the line paths used by all optimal connection graphs for each combination of said slots.

63. (Original) The method of claim 62, wherein the connection graphs are determined to be optimal based on at least one particular selection criterion.

64. (Original) The method of claim 63, wherein the selection criterion is the length of the connection graphs.

65. (Original) The method of claim 64, wherein another selection criterion for determining whether the connection graphs are optimal is the number of bends of the connection graphs.

66. (Original) The method of claim 58, wherein the line paths are defined based on a wiring model for the IC layout and on a partitioning structure defined by the partitioning lines.

67. (Currently Amended) For an electronic-design-automation placer that uses a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions corresponding to said slots, wherein a plurality of edges exist between said slots, a method of pre-computing attributes that are used for ~~costs of~~ placing circuit modules in an IC layout region, the method comprising:

a) for each combination of said slots, identifying at least one connection graph that represents a topology of interconnect lines necessary for connecting the combination of said slots;

b) for each combination of said slots, identifying the edges intersected by the connection graph or graphs for that particular combination of slots, wherein a plurality of the identified edges are diagonal; and

c) storing the plurality of identified edges for each combination of slots in a storage structure, wherein said stored edges are used by the placer to compute costs associated with different placements.

68. (Previously Amended) The method of claim 67, wherein a plurality of the edges are horizontal, and a plurality are vertical.

69. (Original) The method of claim 67, wherein the connection graphs are Steiner trees.

70. (Original) The method of claim 67, wherein the connection graphs are minimum spanning trees.

71. (Original) The method of claim 67, wherein identifying the edges comprises identifying the edges intersected by all optimal connection graphs for each combination of said slots.

72. (Original) The method of claim 71, wherein the connection graphs are determined to be optimal based on at least one particular selection criterion.

73. (Original) The method of claim 72, wherein the selection criterion is the length of the connection graphs.

74. (Original) The method of claim 73, wherein another selection criterion for determining whether the connection graphs are optimal is the number of bends of the connection graphs.

75. (Original) The method of claim 67, wherein the edges are defined based on a wiring model for the IC layout and on a partitioning structure defined by the partitioning lines.